JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH IN EMBEDDED SYSTEMS
EFFECTIVE FROM ACADEMIC YEAR 2022-23 ADMITTED BATCH

R22 COURSE STRUCTURE AND SYLLABUS

I YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core - I	Digital System Design with FPGAs	3	0	0	3
Professional Core - II	System Design with Embedded Linux	3	0	0	3
Professional Elective - I	1. CMOS VLSI Design 2. Pattern Recognition and Machine Learning 3. Wireless Sensor Networks	3	0	0	3
Professional Elective - II	1. Communications Buses & Interfaces 2. Advanced Computer Architecture 3. CMOS Analog IC Design	3	0	0	3
Lab - I	Digital system Design with FPGAs Lab	0	0	4	2
Lab - II	System Design with Embedded Linux Lab	0	0	4	2
	Research Methodology & IPR	2	0	0	2
Audit - I	Audit Course – I	2	0	0	0
	Total	**16**	**0**	8	**18**

I YEAR II – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core - III	ARM Microcontrollers	3	0	0	3
Professional Core - IV	Digital Control Systems	3	0	0	3
Professional Elective - III	1. IoT Architectures and System Design 2. Design for Testability 3. SoC Design	3	0	0	3
Professional Elective - IV	1. Hardware and Software Co-Design 2. Secure Networks 3. Physical Design Automation	3	0	0	3
Lab - III	ARM Microcontrollers Lab	0	0	4	2
Lab - IV	Digital Control Systems Lab	0	0	4	2
	Seminar	0	0	4	2
Audit - II	Audit Course – II	2	0	0	0
	Total	**14**	**0**	**12**	**18**

II YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Elective - V	1. Embedded Networks 2. CMOS Mixed Signal Design 3. Human -Machine Interface	3	0	0	3
Open Elective	Open Elective	3	0	0	3
Dissertation	Dissertation Work Review – II	0	0	12	6
	Total	**6**	**0**	**12**	**12**

II YEAR II - SEMESTER

Course Code	Course Title	L	T	P	Credits
Dissertation	Dissertation Work Review - III	0	0	12	06
Dissertation	Dissertation Viva-Voce	0	0	28	14
	Total	**0**	**0**	**40**	**20**

Open Electives:

1. Business Analytics
2. Industrial Safety
3. Operations Research
4. Cost Management of Engineering Projects
5. Composite Materials

Audit Course I & II:

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development Through Life Enlightenment Skills

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
DIGITAL SYSTEM DESIGN WITH FPGAs (PC – I)

Pre-Requisite: Switching Theory and Logic Design

Course Objectives:

1. To provide extended knowledge of digital logic circuits in the form of state model approach.
2. To provide an overview of system design approach using programmable logic devices.
3. To provide and understand of fault models and test methods.
4. To get exposed to the various architectural features of CPLDS and FPGAS.
5. To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6. To expose software tools used for design process with the help of case studies.

Course Outcomes:

1. To exposes the design approaches using FPGAs.
2. To provide in depth understanding of Fault models.
3. To understands test pattern generation techniques for fault detection.
4. To design fault diagnosis in sequential circuits.
5. To provide understanding in the design of flow using case studies.

UNIT - I

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA technology, architecture, virtex CLB and slice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACT1, ACT2 and ACT3 Architectures. [TEXTBOOK-1]

UNIT - II

Analysis and derivation of clocked sequential circuits with state graphs and tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. Need and Design stratagies for multi-clock sequential circuits. [TEXTBOOK-2]

UNIT - III

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Controller (FSM) – Metastability, Synchronization, FSM Issues, Pipelining resources sharing, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT - IV

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.

Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT - V

Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.3]

TEXT BOOKS

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth, Jr. -5th Ed., Cengage Learning.
3. Digital Circuits and Logic Design-Samuel C. LEE, PHI, 2008.

REFERENCE BOOKS

1. Logic Design Theory-N.N. Biswas, PHI.
2. Digital System Design using programmable logic devices- Parag K. Lala, BS publications.
3. Switching and Finite Automata Theory - Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge, 2010.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
SYSTEM DESIGN WITH EMBEDDED LINUX (PC – II)

Course Objectives:

1. To know the difference between Embedded Linux and Desktop Linux
2. To understand the kernel concepts of Embedded Linux
3. To learn the debugging, writing, profile applications and drivers in embedded Linux.

Course Outcomes: At the end of this course, students will be able to

1. Familiarity of the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Create Linux BSP for a hardware platform

UNIT- I

Introduction to Real Time Operating Systems: Characteristics of RTOS, Tasks Specifications and types, Real-Time Scheduling Algorithms, Concurrency, Inter-process Communication and Synchronization mechanisms, Priority Inversion, Inheritance and Ceiling. Embedded Linux Vs Desktop Linux, Embedded Linux Distributions, System calls, Static and dynamic libraries, Cross tool chains

UNIT- II

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

UNIT- III

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Device Drivers: Communication between user space and kernel space drivers, Character and Block Device Drivers, Interrupt handling, Kernel modules
Embedded Drivers: Serial, Ethernet, I2 C, USB, Timer, Kernel Modules

UNIT- IV

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT- V

Building and Debugging: Bootloaders, Kernel, Root file system, Device Tree

TEXT BOOKS:

1. Chris Simmonds, “Mastering Embedded Linux Programming” - Second Edition, PACKT Publications Limited.
2. Karim Yaghmour, “Building Embedded Linux Systems”, O'Reilly & Associates
3. P Raghvan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design and Development”, Auerbach Publications

REFERENCE BOOKS:

1. Christopher Hallinan, “Embedded Linux Primer: A Practical Real-World Approach”, Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
CMOS VLSI DESIGN (PE - I)

Course Objectives:

1. To understand the concepts of MOS Design and transient response
2. To know the design of combinational MOS logic circuits
3. To know the design of sequential MOS logic circuits
4. To understand the dynamic logic and also memory designing

Course Outcomes: Students will be able to:

1. Design of combinational MOS logic and sequential MOS logic circuits
2. Design of different Memories using MOS transistors
3. Design a circuits based on dynamic logic
4. Use CMOS transmission gates in various applications

UNIT - I

MOS Design

Pseudo NMOS logic- Inverter, Inverter threshold voltage, output high voltage, Output lowvoltage, gain at gate threshold voltage, transient response, rise time, fall time, pseudo NMOS logic gates, transistor equivalency, CMOS inverter logic.

UNIT - II

Combinational MOS logic circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates- NOR and NAND gates, Complex logic circuits design- realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full-adder, CMOS transmission gates, designing with transmission gates.

UNIT - III

Sequential MOS logic circuits: Behavior of bistable elements, SR Latch, Clocked Latch and Flip-flop circuits, CMOS D Latch and edge triggered flip-flop.

UNIT - IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, high performance dynamic CMOS circuits.

UNIT - V

Semiconductor Memories: Types, RAM array Organization, DRAM- types, operation, leakage currents in DRAM cell and refresh operation, SRAM - operation, leakage currents in SRAM cells, Flash memory- NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design- Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuit Analysis and Design – Sung Mo Kang, YusufLeblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming Bo Lin,CRC Press, 2011.
2. Digital Integrated Circuits: A Designs Perspective -Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
PATTERN RECOGNITION AND MACHINE LEARNING (PE – I)

Prerequisite: Statistics and Linear Algebra

Course Objectives:

1. The student will be able to understand the mathematical formulation of patterns.
2. To study the various linear models.
3. Understand the basic classifiers.
4. Can able to distinguish different models.

Course Outcomes: On completion of this course student will be able to

1. Familiar the basics of pattern classes and functionality.
2. Construct the various linear models.
3. Use the different kernel methods.
4. Design the Markov and Mixed models.

UNIT-I

Introduction to Pattern recognition: Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization

UNIT-II

Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs, Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models -Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions

UNIT-III

Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity, RVM for classification

UNIT-IV

Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, D-separation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in general graphs, Loopy belief propagation, Learning the graph structure.

UNIT-V

Mixture Models and EM algorithm: K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EM-Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesian linear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.

TEXT BOOKS:

1. Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press, volume no.52.
2. Pattern Recognition and Machine Learning- C. Bishop-Springer,2006.

REFERENCE BOOKS:

1. Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2nd Ed., 2001.
2. The elements of Statistical Learning- Trevor Hastie, Robert Tibshirani, Jerome H. Friedman, Springer, 2nd Ed., 2009.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
WIRELESS SENSOR NETWORKS (PE –I)

Course Objectives

1. To acquire the knowledge about various architectures and applications of Sensor Networks
2. To understand issues, challenges and emerging technologies for wireless sensor networks
3. To learn about various routing protocols and MAC Protocols
4. To understand various data gathering and data dissemination methods
5. To Study about design principals, node architectures, hardware and software required for implementation of wireless sensor networks.

Course Outcomes: Upon completion of the course, the student will be able to:

1. Analyze and compare various architectures of Wireless Sensor Networks
2. Understand Design issues and challenges in wireless sensor networks
3. Analyze and compare various data gathering and data dissemination methods.
4. Design, Simulate and Compare the performance of various routing and MAC protocol

UNIT -I:

Introduction to Sensor Networks, unique constraints and challenges, Advantage of Sensor Networks, Applications of Sensor Networks, Types of wireless sensor networks

UNIT –II

Mobile Ad-hoc Networks (MANETs) and Wireless Sensor Networks, Enabling technologies for Wireless Sensor Networks. Issues and challenges in wireless sensor networks

UNIT –III

Routing protocols, MAC protocols: Classification of MAC Protocols, S-MAC Protocol, B-MAC protocol, IEEE 802.15.4 standard and ZigBee

UNIT -IV

Dissemination protocol for large sensor network. Data dissemination, data gathering, and data fusion; Quality of a sensor network; Real-time traffic support and security protocols.

UNIT -V

Design Principles for WSNs, Gateway Concepts Need for gateway, WSN to Internet Communication, and Internet to WSN Communication. Single-node architecture, Hardware components & design constraints, Operating systems and execution environments, introduction to TinyOS and nesC.

TEXT BOOKS:

1. Ad-Hoc Wireless Sensor Networks- C. Siva Ram Murthy,B. S. Manoj, Pearson
2. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE

REFERENCE BOOKS:

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Wireless Communication and Networking – William Stallings, 2003, PHI.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
COMMUNICATION BUSES AND INTERFACES (PE - II)

Course Objectives:

1. To know how to select the suitable Buses for different applications
2. To know the architecture of CAN and applications
3. To understand the use of PCIe, USB etc.,
4. To know the serial communication protocol

Course Outcomes: At the end of the course, students will be able to:

1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

UNIT - I

Serial Busses - Physical interface, Data and Control signals, features, limitations and applications of RS232, RS485, I2C, SPI

UNIT - II

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT - III

PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT - IV

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT - V

Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable

TEXT BOOKS:

1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems”, Lakeview Research, 2nd Edition
2. Jan Axelson, “USB Complete”, Penram Publications
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
4. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 –200x
6. Technical references onwww.can-cia.org, http://www.pcisig.com/www.pcisig.com, http://www.usb.org/www.usb.org

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
ADVANCED COMPUTER ARCHITECTURE (PE – II)

Course Objectives:

1. To understand the fundamental of computer design
2. To know the pipelines and parallelism concepts
3. To know the issues in interconnect networks

Course Outcomes: At the end of the course, students will be able to:

1. Familiarize the instruction set, memory addressing of Computer
2. Handle the issues in pipelining and parallelism
3. Familiarize the practical issues in inter network

UNIT - I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT - II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT - IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT - V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, “Modern Processor Design: Fundamentals of Super Scalar Processors”, 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., “Computer Architecture and Parallel Processing”, Mc Graw Hill.
3. DezsoSima, Terence Fountain, Peter Kacsuk, “Advanced Computer Architecture - A Design Space Approach”, Pearson Education.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
CMOS ANALOG IC DESIGN (PE -II)

Pre-requisite: Analog Electronics

Course Objectives: Analog circuits play a very crucial role in all electronic systems and due to continuedminiaturization, many of the analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS analog Ics.
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved in theMOS transistor level design common to all analog CMOS ICs.
3. To understand specific design issues related to single and multistage voltage, current anddifferential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and OP AMPs.

Course Outcomes: After studying the course, each student is expected to be able to

1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various amplifiers like differential, current and operational amplifiers.

UNIT - I
MOS Devices and Modeling
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small- Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT- II
Analog CMOS Sub-Circuits
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT – III
CMOS Amplifiers
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT - IV
CMOS Operational Amplifiers
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps,Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT - V
Comparators
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford UniversityPress, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
DIGITAL SYSTEM DESIGN WITH FPGAs LAB (Lab – I)

Part –I:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of Full Adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of Combinational circuit using Decoders.
4. Design of Combinational circuit using encoder (without and with parity).
5. Design of Combinational circuit using multiplexer.
6. Design of 4 bit binary to gray converter using MUX or Decoders.
7. Design of Multiplexer/ Demultiplexer, comparator in all 3 styles.
8. Modelling of an Edge triggered and Level triggered FFs : D, SR, JK
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
10. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out using different FFs.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier, Divider.
13. Design of ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment,
14. Implementing the above designs on FPGA kits.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
SYSTEM DESIGN WITH EMBEDDED LINUX LAB (Lab – II)

List of Experiments:

1. **Functional Testing Of Devices:** Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems:** Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430:** Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity:** Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. **Battery Voltage Range Indicator:** Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)
7. **Dice Game Simulation:** Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface:** Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device:** Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board:** Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.
11. **Webcam Server:** Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission:** Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note: Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
RESEARCH METHODOLOGY AND IPR

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT- I:
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.
Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT- II:
Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT- III:
Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT- IV:
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT- V:
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science & engineering students’”
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”
2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007.
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.
7. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
ARM MICROCONTROLLERS (PC -III)

Prerequisite: Microprocessors and Microcontrollers

Course Objectives:

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

Course Outcomes: After completing this course the student will be able to:

1. Explore the selection criteria of ARM processors by understanding the functional level trade off issues.
2. Explore the ARM development towards the functional capabilities.
3. Work with ASM level program using the instruction set.
4. Programming the ARM Cortex M.

UNIT - I

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT - II

Introduction to the Arm Instruction Set: Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT - III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors- Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT - IV

Instruction SET of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT -V

Floating Point Operations About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXT BOOKS:

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT- ARM System Developer's Guide Designing and Optimizing System Software, Elsevier Publications, 2004.
2. Joseph Yiu, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Elsevier Publications, 3rd Ed.,

REFERENCE BOOKS:

1. Steve Furber - Arm System on Chip Architectures –Edison Wesley, 2000.
2. David Seal - ARM Architecture Reference Manual, Edison Wesley, 2000.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
DIGITAL CONTROL SYSTEMS (PC -IV)

Prerequisite: Control Systems

Course Objectives:

1. To understand the fundamentals of digital control systems representations, z-transforms
2. To understand analysis of discrete complex domain: Z-Transforms
3. To understand the concepts of state variables analysis for discrete LTIV systems.
4. To understand the concepts of controllability and observability of discrete time systems
5. To get exposed the design aspects of controllers and for discrete time systems
6. To understand the concepts of the stability for discrete LTIV systems
7. To understand the design aspects of observers for discrete time systems.

Course Outcomes: At the end of this course, students will demonstrate the ability to

1. Obtain discrete representation of LTI systems.
2. Find the state space analysis of discrete time systems.
3. Test and analyze the controllability and observability for discrete time systems
4. Analyze stability of discrete time systems using various methods
5. Design and analyze digital controllers.
6. Design state feedback controllers and observers.

UNIT- I: REPRESENTATION OF DISCRETE TIME SYSTEMS

Basics of Digital Control Systems. Discrete representation of continuous systems. Sample and hold circuit. Mathematical Modeling of sample and hold circuit. Effects of Sampling and Quantization. Choice of sampling frequency. ZOH equivalent.

Z-Transforms, Mapping from s-plane to z plane, Properties of Z-Transforms and Inverse Z Transforms. Pulse Transfer function: Pulse transfer function of closed loop systems. Solution of Discrete time systems. Time response of discrete time system, Steady State errors.

UNIT- II: DISCRETE TIME STATE SPACE ANALYSIS

State space representation of discrete time systems, Conversion of pulse transfer function to state space models and vice-versa, Solving discrete time state space equations, State Transition Matrix, Pulse Transfer Function Matrix. Discretization of continuous time state space equations. Concept of Controllability, stabilizability, observability, reachability – Controllability and observability tests. Effect of pole zero cancellation on the controllability & observability.

UNIT- III: STABILITY ANALYSIS OF DISCRETE TIME SYSTEM

Concept of stability in z-domain, Stability analysis discrete time system: by Jury test, using bilinear transformation.Stability Analysis of discrete time systems using Lyapunov methods.

UNIT- IV: DESIGN OF DIGITAL CONTROL SYSTEM BY CONVENTIONAL METHODS

Design and realization of digital PID Controller, Design of discrete time controllers with bilinear transformation,Design of digital control system with dead beat response, Practical issues with dead beat response design.

UNIT-V: DESIGN STATE FEEDBACK CONTROLLERS AND OBSERVERS

Design of discrete state feedback controllers through pole placement, Design of Discrete Observer for LTI System:Design of full order and reduced observers, Design of observer-based controllers.

TEXT BOOKS:

1. K. Ogata, “Digital Control Engineering”, Prentice Hall, Englewood Cliffs, 1995.
2. M. Gopal, “Digital Control Engineering”, Wiley Eastern, 1988.
3. V, I, George and C. P. Kurian, Digital Control Systems, CENGAGE Learning, 2012

REFERENCE BOOKS:

1. G. F. Franklin, J. D. Powell and M. L. Workman, “Digital Control of Dynamic Systems”, Addison-Wesley,1998.
2. B.C. Kuo, “Digital Control System”, Holt, Rinehart and Winston, 1980.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
IOT ARCHITECTURES AND SYSTEM DESIGN (PE– III)

Course Objectives

1. To Know the definition and basic concepts of IoT
2. Learn the interfacing the IoT and M2M
3. To understand the Architecture of IoT

Course Outcomes: Students will be able to:

1. Integrate the sensors and actuator depending on the applications
2. Interface the IoT and M2M with value chains
3. Write Python programming for Arduino, Raspberry Pi devices
4. Design IoT based systems such as Agricultural IoT, Vehicular IoT etc.,

UNIT - I

IoT introduction: Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT, IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types.

UNIT - II

IoT and M2M: M2M to IoT – A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT.M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies.

UNIT - III

IoT Hands-on: Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino. Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.

UNIT - IV

IoT Architecture: IoT Architecture components, Comparing IoT architectures, A simplified IoT architecture, The core IoT functional stack, IoT data management and compute stack

UNIT - V

IoT System design: Challenges associated with IoT, Emerging pillors of IoT, Agricultural IoT, Vehicular IoT, Healthcare IoT, Smart cities, Transportation and logistics.

TEXT BOOKS:

1. Sudip Misra, Anandarup Mukherjee, Arijit Roy “Introduction to IOT”, Cambridge University Press.
2. David Hanes, Gonzalo salgueiro, Patrick Grossetete, Rob barton, Jerome henry “IoT Fundamentals Networking technologies, protocols, and use cases for IoT”, Cisco Press

REFERENCE BOOKS:

1. Cuno pfister, “Getting started with the internet of things”, O Reilly Media, 2011
2. Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”, 1 st Edition, Apress Publications.
3. “Internet of Things concepts and applications”, Wiley
4. Arshdeep Bahga,Vijay Madisetti “Internet of Things A Hands on approach”, Universities Press

5. Shriram K Vasudevan, RMD Sundaram, Abhishek S Nagarajan, “Internet of things” John Wiley and Sons.
6. Massimo Banzi, Michael Shiloh Make: Getting Started with the Arduino, Shroff Publisher/Maker Media Publishers.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
DESIGN FOR TESTABILITY (PE – III)

Pre-Requisite: Digital System Design

Course Objectives:

1. To acquire the knowledge of fundamental concepts of testing
2. To provide broad understanding the fault simulation.
3. To illustrate the framework of Built-in-self test and Boundary scan methods.

Course Outcomes: Students will be able to

1. Acquire verification knowledge and test evaluation
2. Design for testability rules and techniques.
3. Utilize the scan architectures for different digital circuits.
4. Acquire the knowledge of design of built-in-self test.

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. M.L. Bushnell, V. D. Agrawal, “Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design”, Jaico Publishing House.
2. P. K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
SOC DESIGN (PE – III)

Course Objectives:

1. To learn ASIC design concepts and strategies
2. To know the NISC applications and advantages
3. To familiar with simulation and synthesis process

Course Outcomes: At the end of the course, students will be able to:

1. Identify and formulate a given problem in the framework of SoC based design approaches
2. Design SoC based system for engineering applications
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

UNIT - I

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP)concepts.

UNIT - II

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT - III

Simulation: Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT - IV

Low power SoC design / Digital system Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT - V

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report, analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006

REFERENCE BOOKS

1. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000
2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
HARDWARE AND SOFTWARE CO-DESIGN (PE – IV)

Course Objectives:

1. To Know the Co-design Issues, prototype and emulation techniques
2. To learn Architecture specific techniques
3. To know the different tool for design

Course Outcomes: Students will be able to:

1. Acquire the knowledge on various models of Co-design.
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools during Co-design.
4. Implement validation methods and adaptability.

UNIT - I

Co-Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.
Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,
Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.

REFERENCE BOOKS

1. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, Kluwer Academic Publishers, 2002.
2. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer, 2010

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
SECURE NETWORKS (PE -IV)

Course Objectives:

1. To underlying principles and techniques for network and communication security.
2. To learn practical examples of security problems and principles for countermeasures
3. To provide cryptographic methods, protocols and applications.

Course Outcomes: At the end of the course, students will be able to:

1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.

UNIT -I:

Security: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT -II

Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT -III

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT -IV

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT -V

Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition

REFERENCE BOOKS:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Press,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
PHYSICAL DESIGN AUTOMATION (PE -IV)

Course Objectives:

1. To understand the concepts of Physical Design Process (partitioning, Floor planning etc.,)
2. To know the concepts of design optimization algorithms and their application
3. To understand the clock and power design concepts

Course Outcomes: At the end of the course, students will be able to:

1. Implement automation process for VLSI System design.
2. Familiarize to use various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

UNIT - I

Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT - II

Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, delay models, Layout styles.

UNIT - III

Placement: Problem formulation, classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT - IV

Global routing: Problem formulation, classification of global routing, Maze routing algorithms, Line-Probe algorithms, and shortest path based algorithms, Steiner Tree based algorithms, Integer programming based approach, Performance driven routing.
Detailed Routing: Problem formulation, classification, Single layer, two layer, three layer and Multi-Layer channel routing, Algorithms, Switch box routing.

UNIT - V

Over the Cell Routing - Single layer and two-layer routing: Over the cell routing, Two Layer, Three Layer and Multi-Layer OTC Routing.
Via Minimization: Constraint and Unconstrained via minimization.
Clock and Power Routing: Clocking schemes, design considerations for the clock, Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005,
2. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley& Sons (Asia) Pvt. Ltd.

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
ARM MICROCONTROLLERS LAB (Lab – III)

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
2. Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

List of Assignments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the SysTicktimer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
DIGITAL CONTROL SYSTEMS LAB (Lab – IV)

Perform the following experiments in real time by interfacing with the related hardware.

List of Experiments:

1. PWM pulse generation
2. Three phase voltage monitoring using A/D converter.
3. Three phase current monitoring using A/D converter.
4. Speed monitoring of AC motor.
5. Sine PWM pulse generation.
6. Inverter output voltage control.
7. Control of AC motor using UFD.
8. Control of DC motor using DC drive.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- II YEAR- I SEMESTER
EMBEDDED SYSTEMS
EMBEDDED NETWORKS (PE – V)

Prerequisite: Computer Networks.

Course Objectives:

1. To elaborate on the conceptual frame work of physical layer and topological issues of networking in Embedded Systems.
2. To emphasis on issues related to guided and unguided media with specific reference to Embedded device level connectivity.

Course Outcomes: Student will be able to

1. Acquire knowledge on communication protocols of connecting Embedded Systems.
2. Master the design level parameters of USB and CAN bus protocols.
3. Design Ethernet in Embedded networks considering different issues.
4. Acquire the knowledge of wireless protocols in Embedded domain.

UNIT –I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series -Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari, Cambridge press 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- II YEAR- I SEMESTER
EMBEDDED SYSTEMS
CMOS MIXED SIGNAL DESIGN (PE-V)

Pre-Requisites: Analog Electronics

Course Objectives: The objectives of this course are to

1. Introduce circuit design concepts for basic building blocks used in mixed-signal integrated circuit designs.
2. Provide students with the skills to design mixed-signal integrated circuits with these building blocks.
3. Understand design and operation of basic analog circuits.
4. Know mixed signal circuits like DAC, ADC, PLL etc.
5. Design and analysis of switched capacitor circuits
6. Analysis basic data conversion algorithms and circuits.

Course Outcomes: At the completion of this course, each student will have demonstrated proficiency in:

1. Designing CMOS analog circuits to achieve performance specifications.
2. Analyzing CMOS based switched capacitor circuits.
3. Designing data converters and know how to use these in specific applications
4. Design a mixed-signal circuits with understanding design flow.

UNIT - I
Switched Capacitor Circuits
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT - II
Phased Lock Loop (PLL)
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT - III
Data Converter Fundamentals
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT - IV
Nyquist Rate A/D Converters
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT - V
Oversampling Converters
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013.

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- II YEAR- I SEMESTER
EMBEDDED SYSTEMS
HUMAN MACHINE INTERFACE (PE -V)

Course Objectives:

1. To learn the guidelines for user interface
2. To learn the foundations of Human Computer Interaction
3. To become familiar with the design technologies for individuals and persons with disabilities
4. To learn about different HCI models
5. To become familiar with the features of windows and interactive devices

Course Outcomes: Upon completion of the course, the students will be able to:

1. Design effective dialog for HCI
2. Design effective HCI for individuals and persons with disabilities
3. Assess the importance of user feedback.
4. Explain the HCI implications for designing multimedia/ e-learning Web sites
5. Develop meaningful user interface.

UNIT - I

Basics of User Interface

Importance of user interface- Definition, importance of good design, benefits of good design, brief history of human-computer interface, Graphical User Interface, Popularity of Graphics, Concept of Direct Manipulation, Graphical Systems, Characteristics of GUI, Web user interface popularity, Characteristics and Principles of user interface

UNIT – II

Foundations of Human Computer Interface

The Human: I/O channels – Memory – Reasoning and problem solving; The Computer: Devices – Memory – processing and networks; Interaction: Models – frameworks – Ergonomics – styles – elements – interactivity- Paradigms. - Case Studies

UNIT – III

Design Process

Interactive Design: Basics – process – scenarios – navigation – screen design – Iteration and prototyping. HCI in software process: Software life cycle – usability engineering – Prototyping in practice – design rationale. Design rules: principles, standards, guidelines, rules. Evaluation Techniques – Universal Design

UNIT – IV

Models and Theories

HCI Models: Cognitive models: Socio-Organizational issues and stakeholder requirements, Communication and collaboration models-Hypertext, Multimedia and WWW.

UNIT - V

Windows and Interaction Devices

Window characteristics, Components of window, Window Presentation Style, Types of windows, Organizing window functions, Characteristics of input devices, Selection of proper input devices, Output devices

TEXT BOOKS:

1. Wilbert O. Galitz - The essential Guide to User Interface Design, 3rd Ed.,

2. Wiley, 2007 (Unit I & V)
3. Alan Dix, Janet Finlay, Gregory Abowd, Russell Beale, —Human Computer Interaction‖, 3rd Ed., Pearson Education, 2004 (UNIT II, III & IV)

REFERENCE BOOKS:

1. Daniel Newman, Olivier Blanchard – Human/Machine: The Future of our partnership with machine,
2. Paul R. Daugherty, H. James Wilson – Human+Machine: Reimagining work in the Age of AI Hardcover, Kindle Ed.,

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (EMBEDDED SYSTEMS)

ENGLISH FOR RESEARCH PAPER WRITING (Audit Course - I & II)

Prerequisite: None

Course objectives: Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

UNIT-I:
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II:
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT-III:
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV:
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V:
skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS/ REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (EMBEDDED SYSTEMS)

DISASTER MANAGEMENT (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches,
- planning and programming in different countries, particularly their home country or the countries they work in

UNIT-I:
Introduction:
Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.
Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:
Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:
Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:
Risk Assessment Disaster Risk:
Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT-V:
Disaster Mitigation:
Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, “Disaster Management in India: Perspectives, issues and strategies “’New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.),” Disaster Mitigation Experiences and Reflections”, Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies”, Deep &Deep Publication Pvt. Ltd., New Delhi.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (EMBEDDED SYSTEMS)

SANSKRIT FOR TECHNICAL KNOWLEDGE (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Course Outcomes: Students will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood
- Being a logical language will help to develop logic in students

UNIT-I:
Alphabets in Sanskrit,

UNIT-II:
Past/Present/Future Tense, Simple Sentences

UNIT-III:
Order, Introduction of roots,

UNIT-IV:
Technical information about Sanskrit Literature

UNIT-V:
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS/ REFERENCES:

1. “Abhyaspustakam” – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. “India’s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd., New Delhi.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (EMBEDDED SYSTEMS)

VALUE EDUCATION (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Course outcomes: Students will be able to

- Knowledge of self-development
- Learn the importance of Human values
- Developing the overall personality

UNIT-I:
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II:
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III:
Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV:
Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V:
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS/ REFERENCES:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (EMBEDDED SYSTEMS)

CONSTITUTION OF INDIA (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes: Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

UNIT-I:
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working), **Philosophy of the Indian Constitution:** Preamble**,** Salient Features.

UNIT-II:
Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:
Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:
Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:
Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (EMBEDDED SYSTEMS)

PEDAGOGY STUDIES (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

UNIT-I:
Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT-II:
Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT-III:
Evidence on the effectiveness of pedagogical practices, Methodology for the indepth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV:
Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V:
Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

TEXT BOOKS/ REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.

4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, ‘learning to read’ campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (EMBEDDED SYSTEMS)

STRESS MANAGEMENT BY YOGA (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To achieve overall health of body and mind
- To overcome stress

Course Outcomes: Students will be able to:

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT-I:
Definitions of Eight parts of yog. (Ashtanga)

UNIT-II:
Yam and Niyam.

UNIT-III:
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT-IV:
Asan and Pranayam

UNIT-V:
i) Various yog poses and their benefits for mind & body
ii) Regularization of breathing techniques and its effects-Types of pranayam

TEXT BOOKS/ REFERENCES:

1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (EMBEDDED SYSTEMS)

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes: Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT-I:

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT-II:

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT-III:

Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT-IV:

Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V:

- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.