



GLOBAL INSTITUTE OF ENGINEERING & TECHNOLOGY

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Survey No. 179, Chilkur (V), Moinabad (M), Ranga Reddy Dist. TS.

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JNTUH Code(U6) CIVIL - CSE - MECH - ECE - EEE - MBA - M.Tech. EAMCET Code-GLOB

Department of Electronics and Communication Engineering

Mr.CH.Sreedhar
B.Tech.,M.Tech.,
Assistant Professor & Head

Date: 24/10/2014

CIRCULAR

The Department of Electronics and Communication Engineering is hosting for *A Three Day Refresher Course on Real time DSP System Design, Coding & Optimization* for the students of B. Tech.(ECE) in Room No. 04 from 06th November 2014 to 08th November 2014 . All the students of B.Tech (ECE) are hereby informed to register for the course on or before 02nd November 2014. The Co-Ordinator for the course is Mr.G Ahmed Zeeshan, Assistant Professor, Department of ECE.

HEAD

Department of Electronics & Communication Eng
Global Institute of Engineering & Technolog
Chilkur (V), Moinabad (M), R.R. Dist.T.S.-50150

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Mentors
Training & Placement Cell
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

A Three Day Refresher Course


On

Real Time DSP system Design, Coding & Optimization

(06th -08th November, 2014)

PROGRAMME SCHEDULE

	TIME	SESSION	SPEAKER
Day 1	9:30 AM - 10:00 AM	Inauguration	
	10:00 AM - 11:00 AM	Introduction to Real time DSP	Mr.CH.Sreedhar, Asst.prof & Head, Dept.of ECE
	11:00 AM - 11:30 AM	HIGH TEA	
	11:30 AM - 01:00 PM	Hardware & Software Design issues for DSP	Mr.G Ahmed Zeeshan, Asst.prof, Dept. Of ECE
	01:00 PM - 02:00 PM	LUNCH BREAK	
	02:00 PM - 03:30 PM	DSP system Design flow	Mr.Zaheeruddin, Technical Lead, Data Point Pvt.Ltd.
	Day 2	09:30 AM - 11:00 AM	DSP Coding Tools and Algorithms
11:00 AM - 11:15 AM		TEA BREAK	
11:15 AM - 01:00 PM		Measuring the DSP code performance	Mr.G Ahmed Zeeshan, Asst.prof, Dept. Of ECE
01:00 PM - 02:00 PM		LUNCH BREAK	
02:00 PM - 03:30 PM		Optimized implementation of DSP	Mr.CH.Sreedhar, Asst.prof & Head, Dept.of ECE
Day 3		09:30 AM - 11:00 AM	Code Optimization process
	11:00 AM - 11:15 AM	TEA BREAK	
	11:15 AM - 01:00 PM	DSP Operating systems	Mr. Venkatesh, Engineer, Capricot Technologies Pvt.Ltd.
	01:00 PM - 02:00 PM	LUNCH BREAK	
	02:00 PM - 03:30 PM	Valedictory Function , Feedback and Certificate Distribution	


Coordinator
 Mr.G Ahmed Zeeshan
 Assistant Professor
 Department of ECE



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING A Three Day Refresher Course

On

Real Time DSP system Design, Coding & Optimization

(06th-08th November 2014)

LIST OF PARTICIPANTS

S. NO:	NAME OF THE PARTICIPANT
1.	AKULA VINELA
2.	ARAVELLI SHIVAVARDHAN RAO
3.	ARVATI CHAMESWARI
4.	B MONICA
5.	BIRLA JYOTHI SWAROOP
6.	D RAJESH KUMAR
7.	DUGYALA VIJENDER
8.	E VENKATESH
9.	ENGILI MAHENDAR
10.	GANGULA REVANTH SAI
11.	GANGULAWAR NARESH
12.	GOURAGARI SHALINI
13.	GOVU CHENDRASHEKAR
14.	GUMUDAVELLY VIKAS KUMAR
15.	K.SAI KIRAN
16.	KALE RAVI KUMAR
17.	KANCHALA RAVI
18.	KATKAR PRIYANKA
19.	KIRAN KUMAR GADDAM
20.	LOKA PRASHANTH
21.	MADHAVI SINGARI
22.	MANGALI VIJAYALAXMI
23.	MD. JAHIRUDDIN
24.	MOHD ABDUL JAMEEL
25.	PANNALA NIVAS
26.	PAVADALA SANTHOSH
27.	POTHARAJU KUMARASWAMY
28.	S.P MOUNIKA
29.	VANGA SHYAMSUNDAR
30.	VATTEM SAIABHILASH
31.	Y MOHD FARHAN
32.	M NIRANJAN
33.	V GOPAL

Red
06/11/2014
Co-Ordinator
Mr. G Ahmed Zeeshan
Assistant Professor
Department of ECE



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REGISTRATION FORM


(Please Fill in CAPITAL LETTERS)

Name : B. MONICA
Roll No : 11U61A0404
Course/Year : B. TECH IVth Yr
Department : ECE
E-mail : monica53@gmail.com
Phone No : 9985195263


Signature of Participant

For Office use only

Approved/ Not Approved


Signature of Coordinator



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ATTENDANCE SHEET

S.No.	Name of the Participant	Programme	Year	Signature										
				Day-1 (06/11/2014)			Day-2 (07/11/2014)			Day-3 (08/11/2014)				
				FN	AN	AN	FN	AN	FN	AN	FN	AN		
1.	AKULA VINELA	B.Tech	IV	A Vinela	A Vinela	A Vinela	A Vinela	A Vinela	A Vinela	A Vinela	A Vinela	A Vinela	A Vinela	A Vinela
2.	ARAVELLI SHIVAVARDHAN RAO	B.Tech	IV	ASR	ASR	ASR	ASR	ASR	ASR	ASR	ASR	ASR	ASR	ASR
3.	ARVATI CHAMESWARI	B.Tech	IV	Chamela	Chamela	Chamela	Chamela	Chamela	Chamela	Chamela	Chamela	Chamela	Chamela	Chamela
4.	B MONICA	B.Tech	IV											
5.	BIRLA JYOTHI SWAROOP	B.Tech	IV	Swaroop	Swaroop	Swaroop	Swaroop	Swaroop	Swaroop	Swaroop	Swaroop	Swaroop	Swaroop	Swaroop

Co Ordinator

Head of the Department

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				FN	AN	FN	AN	FN	AN	FN	AN	FN	AN		
6.	D RAJESH KUMAR	B.Tech	IV	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>	<i>Rajesh</i>
7.	DUGYALA VIJENDER	B.Tech	IV	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>	<i>Vijender</i>
8.	E VENKATESH	B.Tech	IV	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>	<i>Venkatesh</i>
9.	ENGILI MAHENDAR	B.Tech	IV	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>	<i>Mahendar</i>
10.	GANGULA REVANTH SAI	B.Tech	IV	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>	<i>Revanth</i>

[Signature]

Co Ordinator

[Signature]

HEAD
 Department of Electronics & Communication Engg.
 Global Institute of Engineering & Technology
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[Signature]

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				FN	AN	FN	AN	FN	AN	FN	AN	FN	AN
11.	GANGULA WAR NARESH	B.Tech	IV	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
12.	GOURAGARI SHALINI	B.Tech	IV	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
13.	GOVU CHENDRASHEKAR	B.Tech	IV	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
14.	GUMUDAVELLY VIKAS KUMAR	B.Tech	IV	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
15.	K.SAI KIRAN	B.Tech	IV	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>

[Signature]
 Co Ordinator

[Signature]
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[Signature]
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				FN	AN	FN	AN	FN	AN	FN	AN	FN	AN
16.	KALE RAVI KUMAR	B.Tech	IV	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>
17.	KANCHALA RAVI	B.Tech	IV	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>	<i>K.Ravi</i>
18.	KATKAR PRIYANKA	B.Tech	IV	<i>K.Priyanka</i>	<i>K.Priyanka</i>	<i>K.Priyanka</i>	<i>K.Priyanka</i>	<i>K.Priyanka</i>	<i>K.Priyanka</i>	<i>K.Priyanka</i>	<i>K.Priyanka</i>	<i>K.Priyanka</i>	<i>K.Priyanka</i>
19.	KIRAN KUMAR GADDAM	B.Tech	IV	<i>K.Gaddam</i>	<i>K.Gaddam</i>	<i>K.Gaddam</i>	<i>K.Gaddam</i>	<i>K.Gaddam</i>	<i>K.Gaddam</i>	<i>K.Gaddam</i>	<i>K.Gaddam</i>	<i>K.Gaddam</i>	<i>K.Gaddam</i>
20.	LOKA PRASHANTH	B.Tech	IV	<i>L.Prasanth</i>	<i>L.Prasanth</i>	<i>L.Prasanth</i>	<i>L.Prasanth</i>	<i>L.Prasanth</i>	<i>L.Prasanth</i>	<i>L.Prasanth</i>	<i>L.Prasanth</i>	<i>L.Prasanth</i>	<i>L.Prasanth</i>

Sudh
 Co Ordinator

Prashanth
 Head of the Department

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21.	MADHAVI SINGARI	B.Tech	IV	<i>M. G. S. S. S.</i>	<i>M. G. S. S. S.</i>	<i>M. G. S. S. S.</i>	<i>M. G. S. S. S.</i>	<i>M. G. S. S. S.</i>	<i>M. G. S. S. S.</i>	<i>M. G. S. S. S.</i>	<i>M. G. S. S. S.</i>	<i>M. G. S. S. S.</i>
22.	MANGALI VIJAYALAXMI	B.Tech	IV	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>
23.	MD. JAHIRUDDIN	B.Tech	IV	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>
24.	MOHD ABDUL JAMEEL	B.Tech	IV	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>
25.	PANNALA NIVAS	B.Tech	IV	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>	<i>Jahiruddin</i>

Jahiruddin
 Co Ordinator

Jahiruddin
 Head of the Department

Jahiruddin
 PR/Principal

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26.	PAVADALA SANTHOSH	B.Tech	IV	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala	Santhosh Pavadala
27.	POTHARAJU KUMARASWAMY	B.Tech	IV	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy	Potharaju Kumaraswamy
28.	S.P MOUNIKA	B.Tech	IV	S.P Mounika	S.P Mounika	S.P Mounika	S.P Mounika	S.P Mounika	S.P Mounika	S.P Mounika	S.P Mounika	S.P Mounika	S.P Mounika	S.P Mounika	S.P Mounika
29.	VANGA SHYAMSUNDAR	B.Tech	IV	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar	Vanga Shyamsundar
30.	VATTEM SAIABHILASH	B.Tech	IV	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash	Vattem Saiabhilash

[Signature]
 Co Ordinator

[Signature]
 Head of the Department

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				FN	AN	FN	AN	FN	AN	FN	AN		
31.	Y MOHD FARHAN	B.Tech	IV	<i>Farhan</i>	<i>Farhan</i>	<i>Farhan</i>	<i>Farhan</i>	<i>Farhan</i>	<i>Farhan</i>	<i>Farhan</i>	<i>Farhan</i>	<i>Farhan</i>	<i>Farhan</i>
32.	M NIRANJAN	B.Tech	IV	<i>Niranjan</i>	<i>Niranjan</i>	<i>Niranjan</i>	<i>Niranjan</i>	<i>Niranjan</i>	<i>Niranjan</i>	<i>Niranjan</i>	<i>Niranjan</i>	<i>Niranjan</i>	<i>Niranjan</i>
33.	V GOPAL	B.Tech	IV	<i>V Gopal</i>	<i>V Gopal</i>	<i>V Gopal</i>	<i>V Gopal</i>	<i>V Gopal</i>	<i>V Gopal</i>	<i>V Gopal</i>	<i>V Gopal</i>	<i>V Gopal</i>	<i>V Gopal</i>

V Gopal
 08/11/2014
 Co Ordinator

V Gopal
 Head of the Department

Department of Electronics & Communication Engg.
 Global Institute of Engineering & Technology
 Chilukur (V), Moinabad (M), R.R. Dist.T.S.-501504

V Gopal
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 PP/Principal
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GLOBAL INSTITUTE OF ENGINEERING & TECHNOLOGY

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JNTUH Code(U6) CIVIL - CSE - MECH - ECE - EEE - MBA - M.Tech. EAMCET Code-GLOB

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

A Three Day Refresher Course

On

Real Time DSP System Design, Coding & Optimization

(06th-08th November, 2014)

FEEDBACK FORM

Please valuate your rating of the course by placing a tick in the appropriate box.

1. Poor 2. Satisfactory 3. Good 4. Very good 5. Excellent

Branch and Year: *ECE IV*

Date: *8/11/2014*

ASPECTS	RATING				
	Excellent 5	Very good 4	Good 3	Satisfactory 2	Poor 1
Relevance of contents	✓				
Trainer was knowledgeable and skillful	✓				
Quality of input provided	✓				
Quality of presentations		✓			
Adherence to the time schedule		✓			
Opportunity given to participant to clear doubts	✓				
Identify ways to build on current skills and knowledge	✓				
Overall learning experience	✓				
How has the course enhanced your skills or understanding of this topic?					
<i>I am more confident about the dsp, which is one of the core areas in ECE</i>					
Specify problems faced by you during the course?					
<i>-NIL-</i>					

REPORT
ON
THREE DAY REFRESHER COURSE:
REAL TIME DSP SYSTEM DESIGN, CODING &
OPTIMIZATION
HELD AT
GLOBAL INSTITUTE OF ENGINEERING AND
TECHNOLOGY, HYDERABAD
(06th -08th November, 2014)

A Three day refresher course titled “REAL TIME SYSTEM DESIGN, CODING & OPTIMIZATION” was organized by department of Electronics & Communication Engineering OF GIET ,HYDERABAD the course commenced with inaugural ceremony at 9:30 AM Mr.CH.Sreedhar, Assistant Professor & Head of ECE, GIET. Welcomed all the dignitaries present on the dais and colleagues & students. He mentioned about the significance of the course. Mr.G Ahmed Zeeshan, Assistant Professor of ECE , GIET described the importance of Digital Signal Processing in electronics and communication engineering and how they are interconnected from a long time. He motivated everyone to actively participate in the refresher course to get benefited.

Day 1: The Technical session started at 10:00 am, Mr.CH.Sreedhar, Assistant Professor & Head of ECE, GIET. Delivered a topic on “Introduction to Real Time DSP”. He discussed the basics of Digital Signal Processing and how it can be used in real time and embedded system design. Mr.G. Ahmed Zeeshan, Assistant Professor, GIET explained the “Hardware & Software Design issues for DSP” such as the issues involved in the system level design of real time DSP systems, particularly high performance multiple processor systems from 11:30 AM to 1:00 PM. The next speaker Mr. Zaheeruddin, Technical Lead, Data Point Pvt.Ltd., Hyd. lectured on “DSP system design flow” which includes applying good high speed design practices which are necessary to minimize both component and system related noise to ensure system design success. He discussed design flow steps involved in designing DSP from 2:00 PM to 3:30 PM.

Day 2: Session started at 9:30 am, Mr. Zaheeruddin, Technical Lead, Data Point Pvt.Ltd., delivered lecture on “DSP Coding Tools and Algorithms”.He discussed the code generation tools and DSP development tools. Mr.G Ahmed Zeeshan, Assistant professor GIET explained the “Measuring the DSP code performance” which includes different ways involved in the measuring the DSP performance like memory usage, energy consumption etc. The next speaker Mr.CH. Sreedhar, Assistant Professor & Head of ECE, GIET. Delivered a topic on “Optimized implementation of DSP”. He has given detail description about implementation using structured models and different systematic methods involved in designing of DSP from 2:00 PM to 3:30 PM.

REPORT

Day 3: Session was started at 9:30 AM chaired by Mr. Venkatesh, Engineer, Capricot Technologies Pvt.Ltd., delivered two lectures on “Code Optimization process” & “DSP Operating systems”. He discussed processing steps involved in code optimization process and architectural features. Followed by the DSP applications must respond quickly to many external events, be able to prioritize processing, and perform many tasks at once. The refresher concludes with validatory function, feedback and certificate distribution.

APJAL INSTITUTE OF ENGINEERING AND TECHNOLOGY, HYDERABAD

Handwritten signature
Co Ordinator

Mr. G Ahmed Zeeshan

Assistant Professor

Department of ECE

(06th -08th November, 2014)

A The course titled "REAL TIME SYSTEM DESIGN, CODING & OPTIMIZATION" was organized by department of Electronics & Communication Engineering OF GIT, HYDERABAD the course commenced with inaugural ceremony at 9:30 AM Mr. CH. Sreedhar, Assistant Professor & Head of ECE, GIT, Hyderabad all the dignitaries present on the date and colleagues & students. He mentioned about the significance of the course. Mr. G. Ahmed Zeeshan, Assistant Professor of ECE, GIT, described the importance of Digital Signal Processing in electronics and communication engineering and how they are interconnected from a long time. He motivated everyone to actively participate in the refresher course to get benefited.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

A Three Day Refresher Course

On

REAL TIME DSP SYSTEM DESIGN, CODING & OPTIMIZATION
(06th – 08th November 2014)

CERTIFICATE OF PARTICIPATION

This is to certify that Ms./Mr. K. Priyanka
bearing roll number 11UG1A0421 has attended a Three Day Refresher Course on "REAL TIME DSP SYSTEM DESIGN, CODING & OPTIMIZATION" held from 06th November 2014 to 08th November 2014 at Global Institute of Engineering and Technology.

Coordinator
(Mr G Ahmed Zeeshan)

Head of the Department
(Mr. CH Sreedhar)

Principal
(Dr. Mrs. Ravindra Tiwari)



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

A Three Day Refresher Course

On

REAL TIME DSP SYSTEM DESIGN, CODING & OPTIMIZATION
(06th – 08th November 2014)

CERTIFICATE OF PARTICIPATION

This is to certify that *Ms./Mr.* Loka. Prashanth
bearing roll number 11UGIA0423 has attended a Three Day Refresher Course on "REAL TIME DSP SYSTEM DESIGN, CODING & OPTIMIZATION" held from 06th November 2014 to 08th November 2014 at Global Institute of Engineering and Technology.

Coordinator

(Mr G Ahmed Zeeshan)

Head of the Department

(Mr.CH Sreedhar)

Principal

(Dr. Mrs. Ravindra Tiwari)



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

A Three Day Refresher Course

On

REAL TIME DSP SYSTEM DESIGN, CODING & OPTIMIZATION
(06th – 08th November 2014)

CERTIFICATE OF PARTICIPATION

This is to certify that *Mrs./Mr.* Grangula Revanth Sai
bearing roll number 11U61A0415 has attended a Three Day Refresher Course on "REAL TIME DSP SYSTEM DESIGN, CODING & OPTIMIZATION" held from 06th November 2014 to 08th November 2014 at Global Institute of Engineering and Technology.

Coordinator

(Mr G Ahmed Zeeshan)

Head of the Department

(Mr.CH Sreedhar)

Principal

(Dr. Mrs. Ravindra Tiwari)